Via Hole Studies on a Monolithic 2–20 GHz Distributed Amplifier

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Abstract—**The role of source inductance on the performance of a distributed amplifier is investigated. A simple theoretical analysis shows that optimum performance is obtained with as low a source inductance as possible (as would be intuitively expected), and that the flattest gain and minimum gate line attenuation occur with the inductance common to the whole amplifier rather than parceled out to each FET individually, as would occur for a MIC distributed amplifier. A novel through-the-wafer via hole process has been developed for a low-inductance contact on monolithic circuits. A 2–20 GHz variable-gate-width monolithic distributed amplifier fabricated with this via-hole grounding technique has demonstrated a 2 dB gain improvement as well as a flatter gain profile compared to that without via grounding. Evidence is presented that indicates that MMIC designs may not be as ideal as expected with regard to being typified by the common inductance case.**

I. Introduction

THE MAIN EFFECTS of source inductance on the performance of a distributed amplifier circuit are increased negative feedback and loss in the gate circuit ($g_m L_s/C_{gs}$), which cause gain deterioration with frequency [1]–[4]. Overall gain is also degraded [5], [6]. A theoretical study with analytical expressions has been derived to investigate these two source inductance effects upon the performance of the distributed amplifier. Depending upon how the amplifier grounding is accomplished (i.e., each FET separately or the amplifier as a whole), it is theoretically shown that the interstage delay of the distributed amplifier can be used to flatten the gain while minimizing the effect of the inductance upon gate-line loss.

With regard to distributed amplifiers, separate grounding of the FET's would be characteristic of hybrid fabrication, while common grounding would be expected to typify MMIC designs. Experimental evidence is presented, however, that seems to indicate that the MMIC approach may be closer to the separate grounding case than would be expected, thereby compromising the gain performance to some degree.

A novel through-the-wafer via hole process using the reactive ion etching technique to form low-inductance contacts on the MMIC amplifier has been developed [7], [8]. A 2–20 GHz monolithic distributed amplifier with five variable-gate-width FET's has been fabricated to study the effect of source inductance on the gain performance of the amplifier. The sources of all FET's are connected as a whole and grounded using either ribbon bonding or the low-inductance via hole grounding. In addition to a flatter gain performance, the amplifier with via hole grounding shows 2 dB higher gain than the amplifier with ribbon grounding.

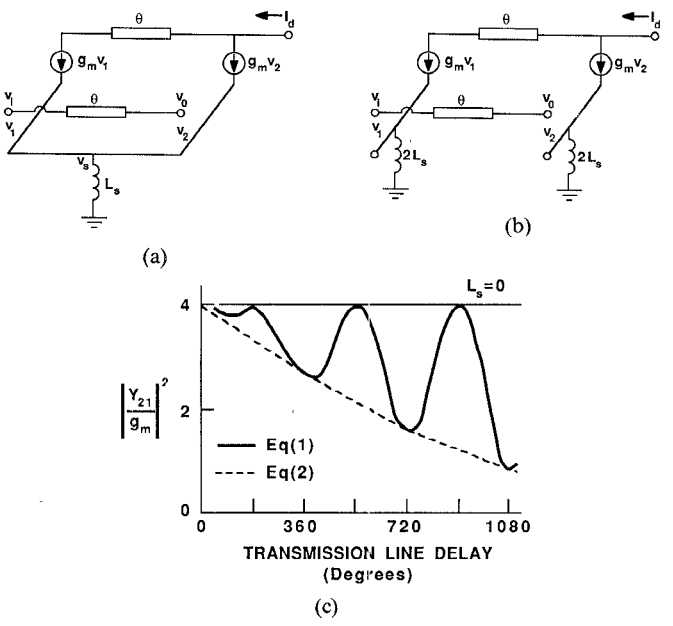

Fig. 1. Gain simulations (c) of the two FET circuits with interstage delays for (a) FET's grounded as a whole or (b) with each FET grounded separately.

II. Theoretical Analysis

The negative feedback effect on the distributed amplifier due to the source inductance is investigated. The analytical expression of the gain for a simple circuit consisting of two parallel FET's with transmission lines connected between the gates and drains of the FET's (as shown in Fig. 1(a)) has been derived as

$$\left|\frac{Y_{21}}{g_m}\right|^2 = \frac{\left[2\cos\theta + \omega L_s g_m(2\sin\theta - \sin 2\theta)\right]^2 + \left[-2\sin\theta - \omega L_s g_m(1-2\cos\theta+\cos 2\theta)\right]^2}{1+(2g_m\omega L_s)^2} \quad (1)$$

where θ is the electrical delay of the lumped transmission line in degrees and L_s is the source inductance. θ is given

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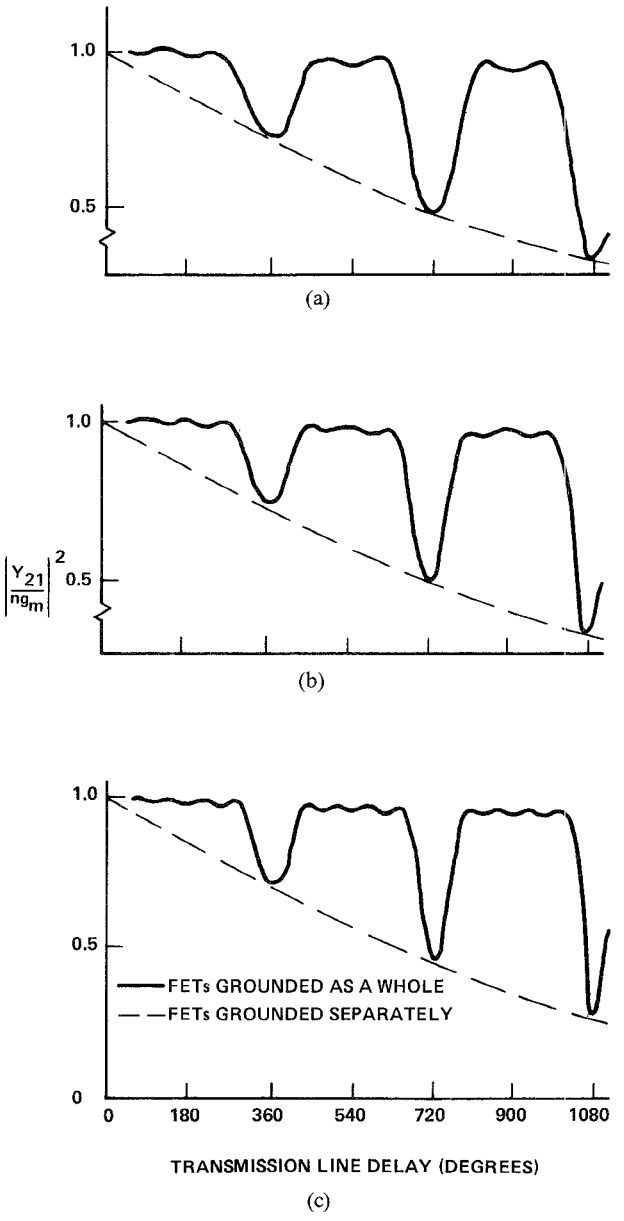

Fig 2. Gain simulations of (a) three, (b) four, and (c) five FET circuits with interstage delays for FET's grounded as a whole or with each FET grounded separately.

by $\cos\theta = 1 - 2(f/f_c)^2$, where f_c is the cutoff frequency of the lumped transmission line. In this derivation, it is assumed that $C_{gs} = 0$ (this is to simulate the distributed amplifier case where the C_{gs} and C_{ds} are incorporated into the 50 Ω artificial transmission lines of the amplifier), that no reflections exist along the transmission lines, and that the two FET's are grounded as a whole.

If the two FET's are grounded separately, as shown in Fig. 1(b), the gain will be the same as the zero delay case which is obtained by setting $\theta = 0$ in (1):

$$\left|\frac{Y_{21}}{g_m}\right|^2 = \frac{4}{1+(2\omega L_s g_m)^2}. \tag{2}$$

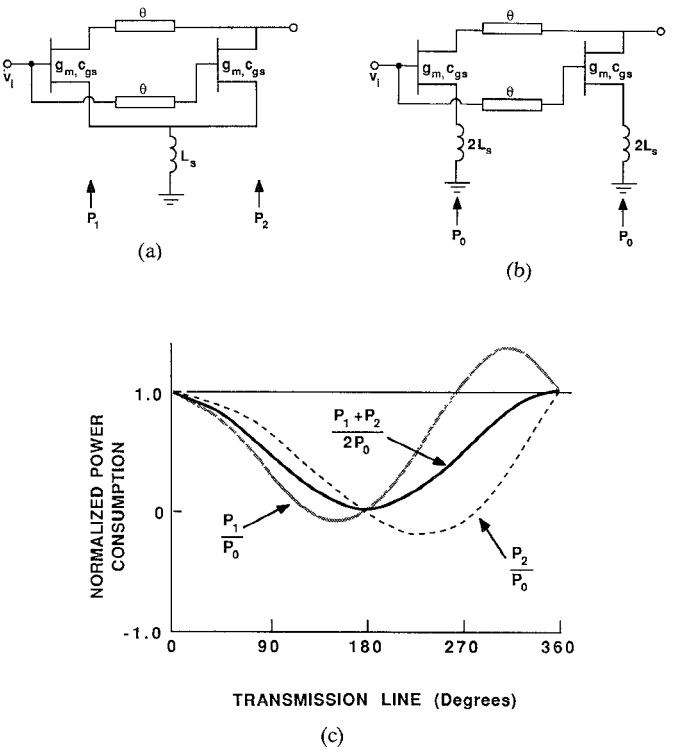

Fig. 3. Normalized power consumptions (c) of each FET and the sum of the two FET's due to source inductance for the circuit shown in (a). The power is normalized to the power consumption of each FET in the circuit (b).

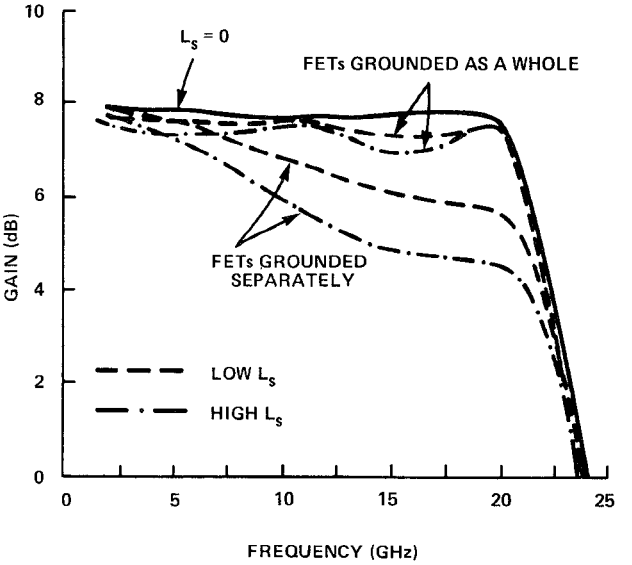

Fig. 4. Gain simulations of a five-FET monolithic distributed amplifier with FET's grounded as a whole or with each FET grounded separately for both low and high source inductances.

Equations (1) and (2) are plotted as a function of θ in Fig. 1(c). Equation (2) is monotonically decreasing with increasing frequency. However, (1) oscillates with a period of 360° between two boundaries, except for a local minimum of magnitude $4[(1+(\omega L_s g_m)^2)/(1+(2\omega L_s g_m)^2)]$ at $\theta = 90°$. The two boundaries correspond to the constant

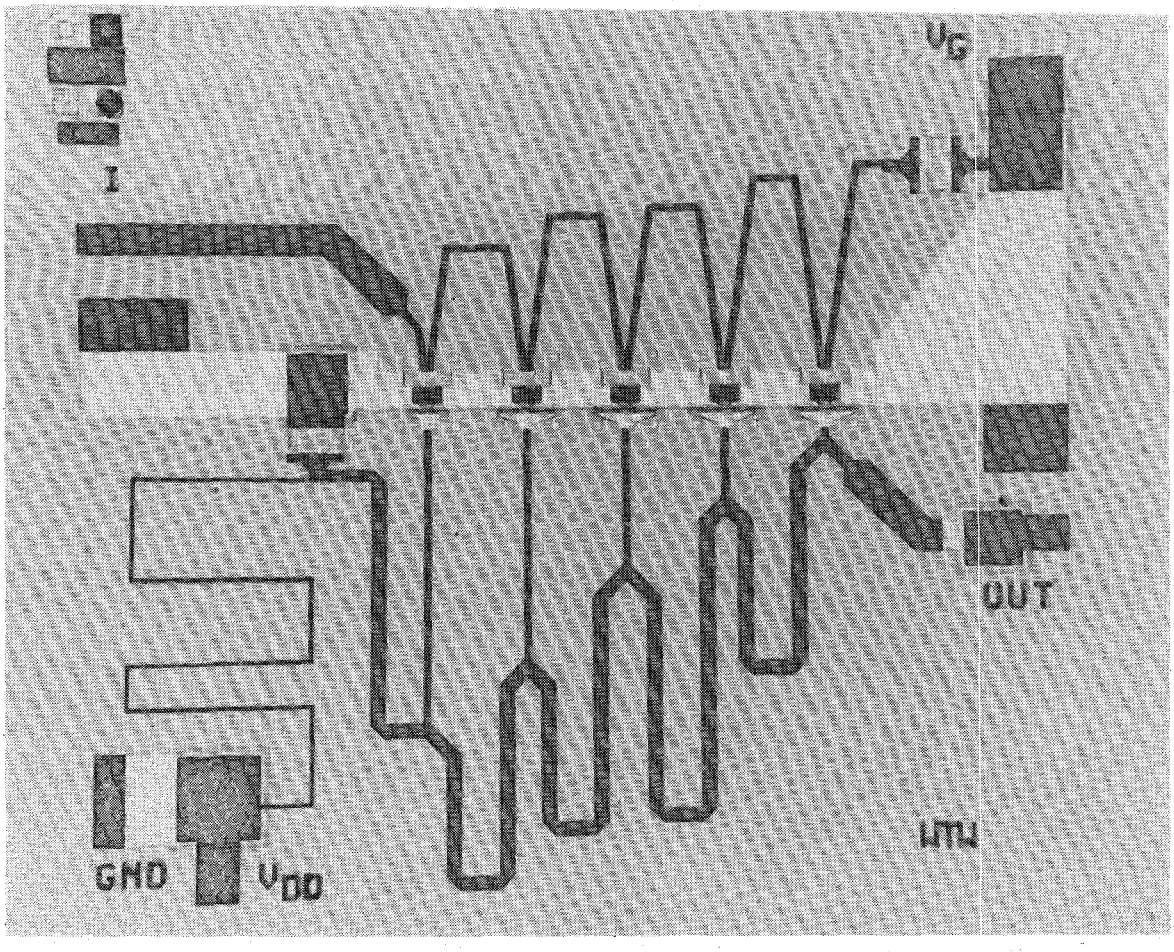

Fig. 5. Photograph of a five-variable FET distributed amplifier chip.

gain with zero source inductance and (2), respectively. For larger source inductance, (2) decays faster with frequency, and the minimum at $\theta = 90°$ is deeper. For a distributed amplifier, θ ranges from 0 to 180° as the frequency ranges from 0 to the cutoff frequency f_c (the upper edge of the amplifier bandwidth).

Supercompact simulation confirms the phenomenon observed in Fig. 1(c). The gain simulations for the same circuits with three, four, and five parallel FET's, respectively, are shown in Fig. 2. For all four circuits, the gain is flattened with frequency if the FET's are grounded together.

The second effect of the source inductance on the distributed amplifier is the equivalent gate resistance, $g_m L_s / C_{gs}$. For the two-FET circuit shown in Fig. 3(b), the power consumption due to this resistance (for each FET, if the FET's are grounded separately) is as follows:

$$P_0 = \frac{2\omega^2 L_s C_{gs} g_m |v_i|^2}{\left(1 - 2\omega^2 L_s C_{gs}\right)^2 + 4\omega^2 L_s^2 g_m^2}. \tag{3}$$

If the two FET's are grounded as a whole (Fig. 3(a)), the power consumptions for the two FET's are different, as shown below (normalized with respect to (3)):

$$\frac{P_1}{P_0} = A_1 - \frac{B_1(1-2a)}{2b} \tag{4}$$

$$\frac{P_2}{P_0} = A_2 - \frac{B_2(1-2a)}{2b} \tag{5}$$

where

$$A_{\frac{1}{2}} = 1 - a(1-\cos\theta) \mp b\sin\theta \qquad a = \omega^2 L_s C_{gs}$$

$$B_{\frac{1}{2}} = b(1-\cos\theta) \mp a\sin\theta \qquad b = \omega g_m L_s.$$

However, the total power consumption of these two FET's is (normalized to $2P_0$)

$$\frac{P_1 + P_2}{2P_0} = \frac{1+\cos\theta}{2} \leqslant 1 \tag{6}$$

which is always lower than the total power consumption when the two FET's are grounded separately, as shown in Fig. 3(c). Therefore, the gate line loss of the distributed amplifier is less if the FET's are grounded together rather than separately. The $g_m L_s$ value used in Fig. 1(c), Fig. 2, and Fig. 3(c) is 9×10^{-12}/Hz.

Fig. 4 shows the comparison of the Supercompact gain simulations for a distributed amplifier consisting of five

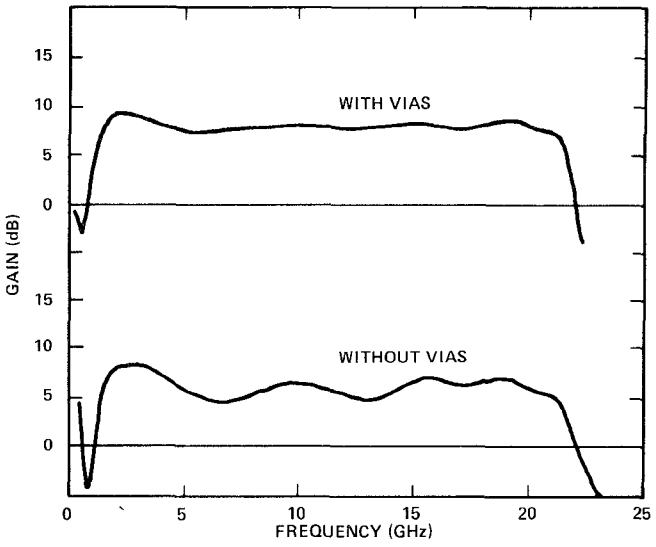

Fig. 6. Comparison of the measured gains between the monolithic distributed amplifiers with via hole grounding and ribbon grounding.

FET's, with each FET grounded separately or with all FET's grounded as a whole. Each simulation includes both low and high source inductance cases, which correspond to $g_m L_s$ values of 9×10^{-12}/Hz and 18×10^{-12}/Hz, respectively. It is clear that the gain is flatter for the amplifier when the FET's are grounded as a whole, and less rippled for the lower source inductance case.

This simple analysis thus shows that flatter gain with minimum gate line attenuation can be achieved with the source inductance common to the whole amplifier, thereby allowing partial cancellation of the out-of-phase currents that flow in the inductor to reduce the virtual size of the inductance. This is the usual case if the amplifier is realized in MMIC form rather than in a MIC where each FET in the amplifier is grounded separately with bond leads. Care must be taken, however, to design the source bus on the MMIC for minimum inductance and resistance along its length.

III. Experiment and Results

A monolithic distributed amplifier design which consists of five FET's with various gate widths and with the sources of all FET's grounded as a whole was developed, as shown in Fig. 5. FET's with a gate length of 0.5 μm and gate widths of 90 μm, 140 μm, 160 μm, 173 μm, and 146 μm were used. Supercompact simulation shows a gain of 7.5 dB and VSWR's of 1.2:1 of the MMIC amplifier over the 2–20 GHz band.

Low-inductance contacts on the MMIC amplifier are realized by using through-the-wafer via holes. A novel process using $SiCl_4/Cl_2$ chemistry with a hard-baked positive resist mask for reactive ion etching of 100-μm-deep via holes in GaAs is developed. The process produces deep vias with relatively smooth sidewalls. A high aspect ratio ($\sim 3:1$) is maintained, but the walls are sufficiently sloped to facilitate the subsequent metallization.

This distributed amplifier was fabricated on MBE material with the choice of using either the low-inductance via hole grounding or higher inductance ribbon grounding. In addition to a flatter gain performance, the amplifier with the via hole grounding has a measured gain of 7.5 ± 0.5 dB, which is 2 dB higher than the same amplifier with the ribbon grounding (as shown in Fig. 6).

IV. Discussion and Conclusions

A theoretical analysis was done showing the importance of grounding the FET's in a distributed amplifier in common rather than separately. A Supercompact simulation confirmed these results, as shown in Fig. 4. Separate grounding of the FET's would be expected to characterize the hybrid realization of the amplifier, while the MMIC realization of the amplifier would be expected to approximate the common mode if a common source bus line were utilized.

Although no empirical results were obtained confirming the improvement of the common mode over the individual mode (there would be no reason to suspect inaccuracies in the CAD simulations for such simple circuit differences), an amplifier run using the common source bus mode showed significant improvement in both gain and ripple through the use of vias in place of ribbon grounding at each end of the bus. This result would be expected because of the lowered inductance of the vias (Fig. 6). Theory says, however, that grounding the FET's in common mode reduces the sensitivity of the gain to large changes in the source inductance (as shown in Fig. 4). It may thus be that the large improvement shown in Fig. 6 is indicative of the lack of complete realization of the common mode. Indeed, simple calculations reveal that the FET-to-FET inductance along the source bus is comparable to the via inductance. (The common mode analysis assumes that this inductance is negligible compared to the via inductance, as was also assumed in the CAD design of the amplifier.)

It thus seems expedient to minimize the source bus inductance further to improve upon the performance shown for the via data in Fig. 6. This will not be trivial, because moving the FET's closer together will raise the via inductance, since their diameter will have to be decreased.

Acknowledgment

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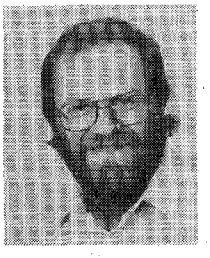

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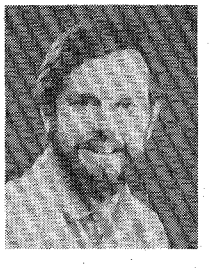

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